

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
MATHEW, LEO, et al.

Application No.: 10/624398

Filed: 7/22/2003

Docket No.: SC12862TC

§ Patent No.: 7013447
§
§ Issue Date: 3/14/2006
§
§ Examiner: Vuthe Sick
§
§ Group Art Unit: 2825
§
§

Title: METHOD FOR CONVERTING A PLANAR TRANSISTOR DESIGN TO A
VERTICAL DOUBLE GATE TRANSISTOR DESIGN

Certificate of Submission

I hereby certify that this correspondence is being submitted to the
USPTO, Alexandria, VA.

- ☐ Addressed per C.F.R. § 1.1(a) and deposited with the United States
Postal Service with sufficient postage as first class mail.
- ☐ Facsimile transmitted in accordance with C.F.R. § 1.6(d).
- ☒ Submitted electronically via EFS in accordance with "Legal
Framework for EFS Web".

January 27, 2007
Date of Submission

Dora Hudgins
Signature

Dora Hudgins
Printed Name of Person Signing Certificate

Commissioner for Patents
Alexandria, VA 22313

SUBMISSION OF CERTIFICATE OF CORRECTION

Dear Commissioner:

Enclosed is a Certificate of Correction listing error(s) in the subject patent. Please enter
these corrections. Since the errors appear to be on the part of the United States Patent Office,
there should be no charge.

1-26-07
Date

Respectfully submitted,

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CERTIFICATE OF CORRECTIONPage 1 of 1

PATENT NO.: 7013447
APPLICATION NO: 10/624398
DATE: 3/14/2006 12:00:00 AM
INVENTOR(S): MATHEW, LEO

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In Column 4, Line 18, Claim No. 1:

Change "or" to -for—

In Column 4, Line 50, Claim No. 7:

Change "tan" to -than—

In Column 4, Line 56, Claim No. 9:

Change "Length" to -length—

MAILING ADDRESS OF SENDER (Please do not use customer number below)

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